MACOM
an AMP company
Corporate R&D Center

100 Chelmsford Street
Lowell, MA. 01853-3294
Ph: 508-656-2626
Fx: 508-656-2777

Naval Research Laboratory
Attn: Dr. Francis J. Kub
Contract Number: N00014-95-C-2022
Code: 6813
4555 Overlook Avenue, SW.
Washington, DC 20375-5326

November 11, 1996

Attention: Dr. Francis J. Kub
Subject: Monthly Progress Report - October, 1996
Reference: SiGe Power HBT

Gentlemen:

1.0 Introduction

The objective of this program is the development and demonstration of a viable SiGe power HBT device design and associated processes that will demonstrate >1 Watt of output power at 6 and 8 GHz.

2.0 Objectives for the Reporting Period

2.1 Complete load-pull characterization of SiGe2 wafer Lot-16 at BSO (2 GHz).

2.2 Complete package assembly and load-pull testing of SiGe2 at PHO (6 GHz).

2.3 Begin load-pull testing of BUR50 wafer lots at BSO (2 GHz) and at PHO (6 GHz).

3.0 Progress During the Reporting Period

3.1 The process runs of both SiGe2 and BUR50 mask sets were completed in September using both the double-polysilicon and polyemitter processes (See Figure 1). The SiGe2 wafers were tested first and exhibited excellent DC probe yield thus making available a large number of chips for evaluation. The breakdown voltage for the 20V material was 18-22 V, and for the 40 V material was 25-30 V.

Based on the measured DC parameters it was determined that the wafers from the double polysilicon process should have the best RF performance and thus were mounted-up onto BeO substrates with bond wires to connect emitter to the input and the base wires to ground as illustrated in Figure 2. A resonant LC bypass was used to to provide an RF ground at the desired operating frequency.

Initial fixture-level power testing (at BSO) of the BeO mounted devices were performed at 1.9 GHz using a load-pull setup. These measurements were limited to low frequencies (below 2 GHz) because of the load-pull test stand inability to tune the input bond wire reactance at higher frequencies; (e.g., 6 GHz). The frequency of 1.9 GHz was chosen to be able to compare the results to other literature-reported SiGe transistor performance. In Class AB operation (Vc = 5 V, Icq = 40-60ma) the device achieved a Po(1dB) ~26 dBm with a gain of >15 dB, and a PAE of >50% (See Fig. 3).

Measurements at 10 V in Class AB demonstrated 1 Watt output power with a gain >15 dB and a power-added efficiency of >50 % (See Fig. 4). These results indicate that the 10 V die will generate the required output power of 1 Watt and have excellent gain and efficiency at 2 GHz. Assuming a 6 dB/octave slope, one should achieve a gain of >10dB at 6 GHz, which should be adequate for good power performance.

Additional 2 GHz testing at CR&D has not been attempted on the SiGe2 wafers; the focus has been on making 6 GHz evaluations. MIM capacitor input matching networks are being used to effect 6 GHz fixture-level testing of the SiGe2 devices (See Figure 5) but a defective coaxial bias-tee has resulted in a delay in further testing at CR&D until a replacement is received.

3.2 Packaged SiGe2 devices have been evaluated at PHO using MIS capacitor input matching networks. Optimization of the matching network continues. Summaries of the test results are shown Tables 1 and 2 and Figure 6.

3.3 Initial testing of packaged BUR50 devices has begun at PHO. Summaries of the test results are shown in Tables 1 and 2.

4.0 Problems and Proposed Solutions

4.1 Trouble shooting and procurement of a replacement for a faulty bias-tee (a cause of instabilities and low frequency oscillations) at CR&D has created delays in 6 GHz measurements.

4.2 Power testing at PHO of the SiGe2 and BUR50 devices at high power levels and particularly in trying to operate in Class-C is resulting in device burnout. This is attributed to the lack of any emitter ballast resistors; an issue that the next mask set will address.

5.0 Objectives for the Next Reporting Period

5.1 Design emitter ballasting for the SiGe2 and BUR50 devices and order mask sets.

5.2 Continue testing of packaged SiGe2 and BUR 50 devices with internal input matching at PHO to obtain full characterization data including load-pull results.

5.3 Obtain new bias-tee and then continue the fixture-level testing at CR&D of SiGe2 and BUR50 devices with input impedance matching at 6 GHz.

Respectfully,

M/A-COM Inc.

B.A. Ziegner
Sr. Principal Engineer

Table 1 DC Parameters

Part	Die	BVces 5mA	BVceo 10ma	BVebo 5ma	Hfe 5V	Hfe@ mA	Re 1.2A	Cob 8V
Y2593	SiGe2	21	12	2.15	80	100		
Y2593	SiGe2	28	11	4	400	100	0.23	2.31
Y2594	SiGe2x3	27	6.5	402	280	100	0.08	
Y2593A	SiGe2	27	15.5	4.5	125	200		
Y2593B	SiGe2	27.5	10.4	5.3	350	100	0.158	
Y2593B								
Y2593B								
Y2593C	SiGe2	27	11		250	100	0.205	
Y2593D	SiGe2							
Y2593E	SiGe2	27	15	3.73	60	100	0.229	
Y2596	BUR51	18	8	4.69	140	100	0.055	7.2
Y2596A	BUR51	17	8	1.71	125	100	0.052	7.6
Y2596B	BUR51 (1cell)	19.4	5.9	5	110	100	0.171	

Table 2 RF Parameters Fo= 5.5 GHz, Class AB, Vcc= 5V

Part	Fres GHz	Gss dB	P1dB dBm	Psat dBm	Zs ohms	Zl ohms	Ic ma	comment
Y2593	none	zero						
Y2594	none							
Y2593A	4.9	16.3	20	23	TBD		120	
Y2593B	5.9	6.5	22.5	24	45 -j15	3.9 -j12.4	92	8V...blew
Y2593B		11.2	18	21.4	95 -j16	3.7 -j13.5	95	
Y2593B		14	20	>22	49 -j72	8.0 -j15	50	
Y2593C	4	9	24	25.4	6.4-j13.5	10.6+j4.5*?	112	8V...blew
Y2593D								
Y2593E	5.2	12.7	18			like Y2593B	115	
Y2596	none	zero						
Y2596A	6.9?	-3					105-300	runaway
Y2596B	6.2	12.3	17	22.8			50	

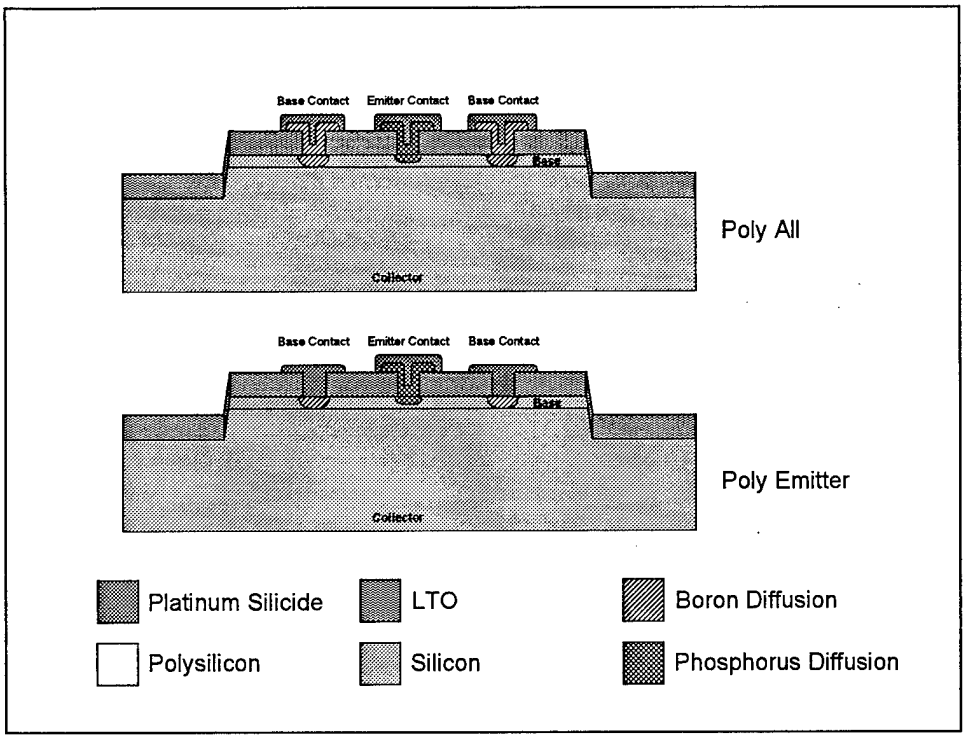

Figure 1 SiGe Device Structures

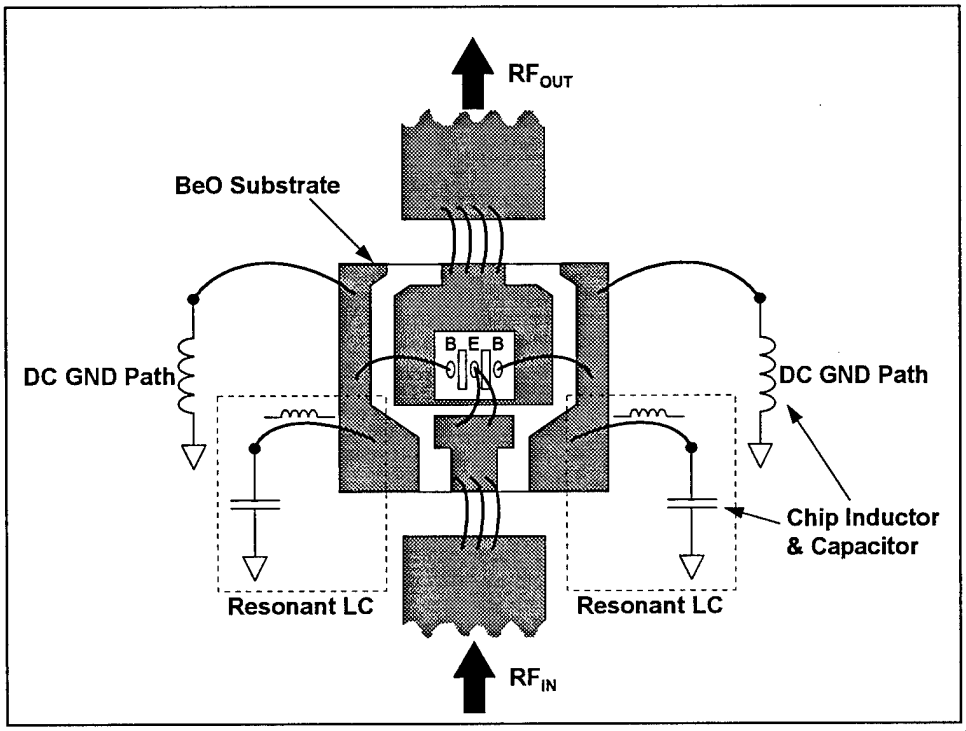

Figure 2 Bonding Diagram of BJT in CR&D Test Fixture @ 1.88 GHz

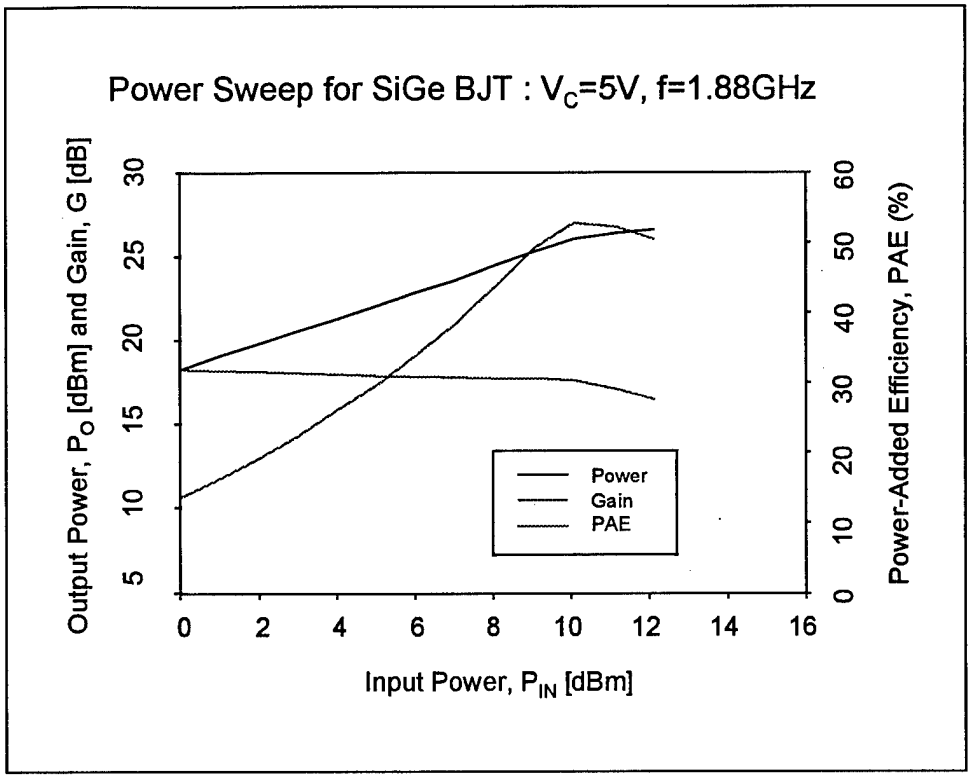

Figure 3 RF Power Sweep Performance at Vc = 5V

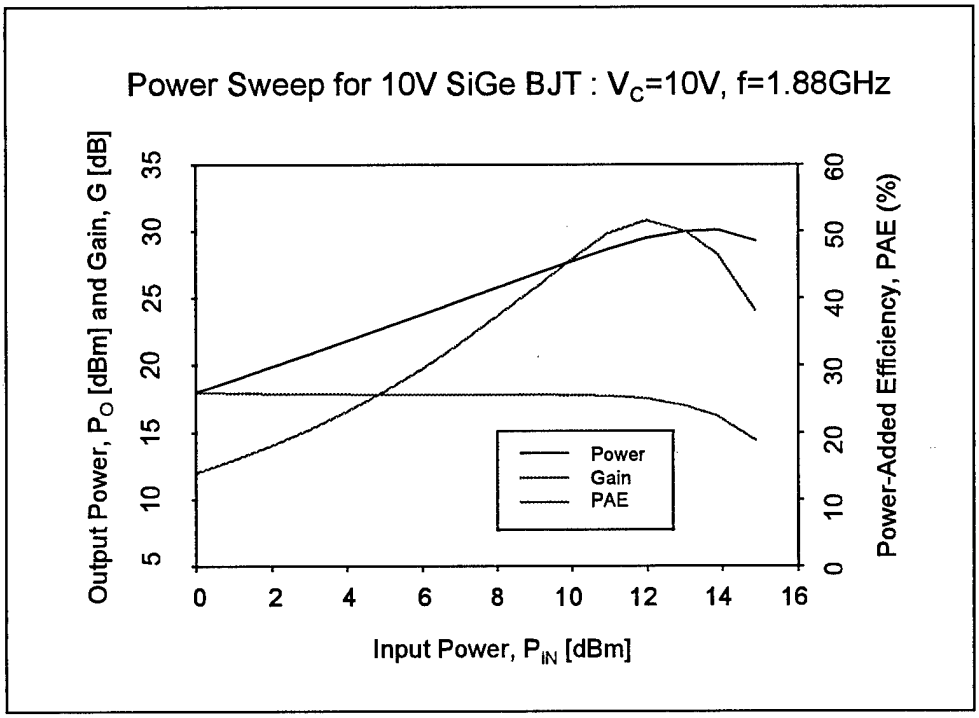

Figure 4 RF Power Sweep Performance at Vc = 10V

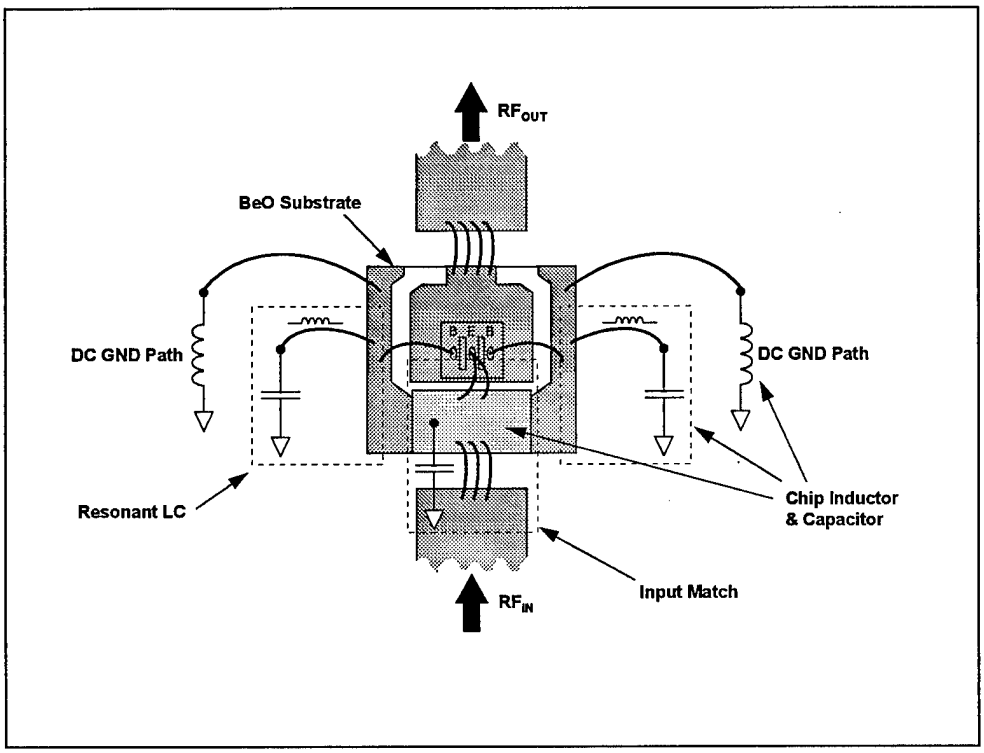

Figure 5 Bonding Diagram of BJT in CR&D Test Fixture @ 6 GHz

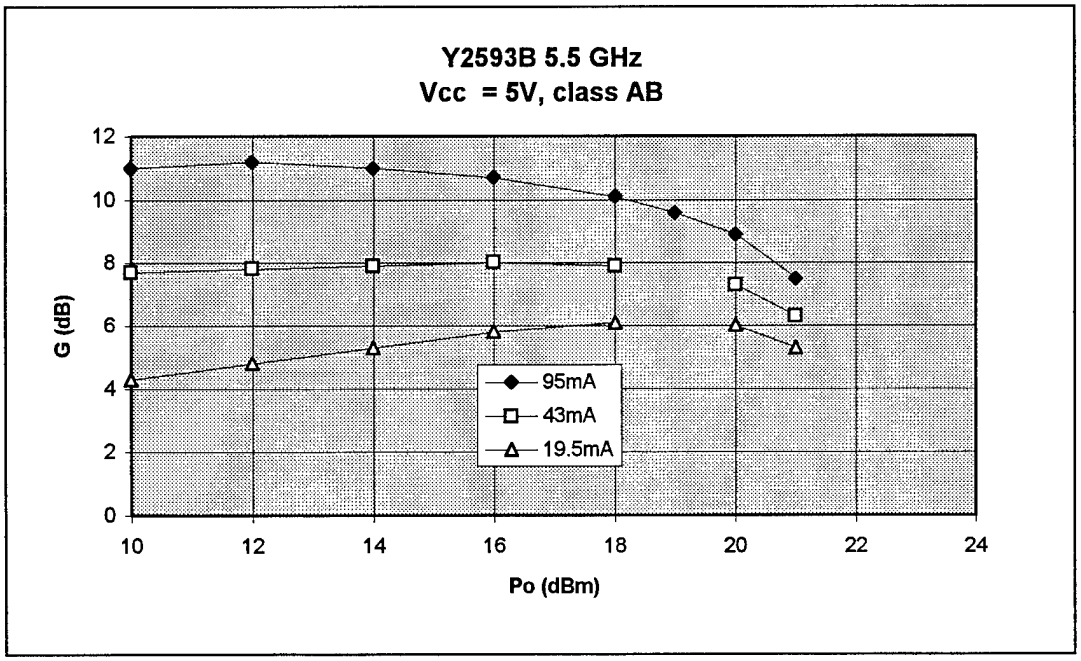

Figure 6 Power Sweep Performance